

CLAIMS:

Sub A1
1. A method of identifying an inaccurate model of a hardware circuit comprising the steps of:

5 simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results;

10 replacing the or each abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

 resimulating the model with said expanded set; and

15 comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

2. A method as claimed in claim 1, wherein the model is an HDL model.

20 3. A method as claimed in claim 2, wherein said plurality of signals are selected from a standard logic package data set comprising one or more simple logic levels and one or more abstract data type levels.

25 4. A method according to claim 3 further comprising the step of, when said abstract data type is an X selected from the standard logic package, expanding each X into a 0 and a 1.

30 5. A method as claimed in claim 3, wherein the or each abstract signal is converted into two simple logic signals.

Sub A2
35 6. A method according to any preceding claim further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with the results from the simulation of an analog model of the circuit, identifying whether the digital model is an accurate model and only comparing the digital model results with the analogue model

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1. The first step is to identify the problem or goal. This involves understanding the current situation and what needs to be achieved.

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means for resimulating the model with said expanded set;

means for comparing the two sets of results and providing

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Sub A3 35

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